REMARKS

Claims 41, 45, 50 and 52 have been amended and claim 53 has been added. Claims 41 and 43-53 are pending in the application. Reconsideration is requested in view of the amendments and the remarks to follow.

Claims 41 and 43-52 stand rejected under 35 U.S.C. §112, first paragraph. Claims 41, 45, 50 and 52 have been amended in response to the concerns noted in the Office Action. Accordingly, the rejection of claims 41 and 43-52 under 35 U.S.C. §112 should be withdrawn, and claims 41 and 43-52 should be allowed.

Claims 41, 45, 46 and 50 stand rejected under 35 U.S.C. §102(b) as being anticipated by Verhaar, U.S. Patent No. 5,015,598, with Hiroki et al., U.S. Patent No. 5,512,771 as evidence, or alternatively, under 35 U.S.C. §103(a). Claims 43 and 47 stand rejected under U.S.C. §103(a) as being unpatentable over Verhaar/Hiroki et al., in view of Pintchovski et al., U.S. Patent No. 5,126,283.

Claims 44, 48, 49, 51 and 52 stand rejected under U.S.C. §103(a) as being unpatentable over Verhaar/Hiroki et al., in view of Pintchovski et al., and further of Brigham et al., U.S. Patent No. 5,714,413, and Kumagai et al., U.S. Patent No. 5,430,313.

Claim 41 recites "after forming the sidewall spacers comprising nitride, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith, wherein a portion of the gate electrode, laterally

adjacent the sidewall spacers and at the interface with the gate dielectric layer, is oxidized", which is not taught, disclosed, suggested or motivated by the cited references, alone or in any proper combination. Claims 45 and 50 also include recitation of oxidation of a portion of the gate.

Verhaar teaches a process whereby a portion of the substrate 10 is oxidized or "regenerated" to form a gate dielectric 11 (see, e.g., Figs. 5-10; text at col. 5, lines 45-52). Verhaar is void of any teaching of oxidizing gate material. In fact, Verhaar explicitly teaches that oxidation is limited to parts of the device "which are not protected by the provisional spacers 20a." (col. 5, lines 28-39). Verhaar teaches optional removal of exposed oxide (col. 3, lines 27-30). Verhaar further teaches (col. 3, lines 31-34) reoxidation being effected "in the lateral direction over a short distance under the spacers" and does not provide any teaching, disclosure, suggestion or motivation to oxidize gate material.

As a result, Verhaar fails to anticipate the invention as recited in the claims (see MPEP §2131). As another result, Verhaar also fails to provide all of the elements recited in the claims, as is required for a finding of unpatentability (see MPEP §706.02(j)).

The Examiner offers an inherency argument, citing In re King, 231 USPQ 136. King deals with an application directed to a method of optical interference that was anticipated by an article of manufacture. In King, the article of manufacture described in the prior art of Donley, U.S. Patent

No. 3,9878,272, necessarily had to function in accordance with the method.

In other words, it was incapable of functioning any other way. "Under the principles of inherency, if a structure in the prior art necessarily functions in accordance with the limitations of a process or method claim of an application, the claim is anticipated."

King attempted to claim physical principles of partial reflection and constructive and destructive interference. As a result, the apparatus cited as anticipating these physical principles could not do anything but what King attempted to claim.

In the instant situation, significant changes in degree of oxidation are possible with variations in numerous parameters, such as: (i) temperature, (ii) oxide thickness, (iii) manner in which the gate dielectric was formed, (iv) oxidation time and a plethora of other variables. As a result, the structure and method taught by Verhaar does not necessarily function in accordance with Applicant's claim. The Examiner is confusing inherency with possibility. In this case, Verhaar explicitly teaches controlling the processing parameters to limit what is and what is not oxidized.

In fact, semiconductor manufacturing is notorious for being sufficiently sensitive to relatively small perturbations in conditions to such an extent that such manufacturers rigorously control processing parameters. Additionally, such manufacturers vigorously test the

processes as well as parts being manufactured to determine when deviations crop up and to remediate such effects immediately.

Accordingly, the Examiner is mistaken in asserting that the burden is shifted to Applicant to prove that inherency does not exist, and, to the extent that any such burden might fall on Applicant, Applicant has successfully rebutted same. Further, Verhaar explicitly teaches controlling these process variables in such a manner to limit oxidation to the area beneath the sidewalls and is careful to show exactly and only this in Figs. 5-10.

Verhaar additionally teaches careful control of the gate edges relative to various portions of the source and drain implants (see Field of the Invention, Background, Summary, Description). Verhaar further teaches that control of oxide thicknesses and gate conductivity are crucial (col. 2, lines 8-17). As a result, Verhaar teaches away from the modifications proposed by the Examiner for multiple reasons (see MPEP §2141.02 and §2145(X)(D)(2)).

Verhaar does not teach oxidation of the gate and further teaches away from oxidation of the gate material. Accordingly, all of the rejections based on Verhaar are prima facie defective and should be withdrawn, and claims 41 and 43-52 should be allowed.

Hiroki et al. teach formation of an oxide layer 6 adjacent a gate structure 5b. In contrast, Applicants recite "forming sidewall spacers comprising nitride on the gate electrode's sidewalls, the sidewall spacers

joining with the gate dielectric layer" (claim 41); "forming sidewall spacers laterally adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls, the sidewall spacers comprising an oxidation resistant material" (claim 45); "forming non-oxide material over the gate structure and the dielectric layer" (claim 50); and "covering a top and sidewalls of the gate structure with an oxidation resistant material" (claim 52).

It is abundantly clear that Hiroki et al. do not teach, disclose, suggest or motivate the invention as recited in any of these claims. This is clear because Hiroki et al. explicitly teach formation of an oxide adjacent the gate material and do so in order to facilitate oxidation of the gate. In other words, Hiroki et al. require a material that (i) is an oxide and (ii) is not oxidation resistant. As a result, it is inconceivable that Hiroki et al. could teach, disclose, suggest or motivate the invention as recited in any of Applicant's claims.

Pintchovski et al. teach a process whereby an Al_2O_3 layer is employed to encapsulate a refractory metal conductor (see, e.g., Abstract). Pintchovski et al. do this in order to optimize conductivity of the conductor by permitting use of pure metal, rather than a silicide or semiconductor materials.

In fact, Pintchovski et al. explicitly teach (col. 1, lines 26-29) that prevention of oxidation of the conductors is a problem to be solved. Pintchovski et al. also explicitly teach (col. 2, lines 38-41) that the layer

inhibits such oxidation. As such, Pintchovski et al. clearly teach away from the invention as recited in any of Applicant's claims.

Not only do Pintchovski et al. explicitly teach away from the invention as recited in any of Applicant's claims, but the intended purpose of Pintchovski et al. is destroyed in attempting to modify the teachings of Pintchovski et al. to try to arrive at the subject matter of Applicant's claims (see MPEP §2143.01). As a result, there is no motivation, as a matter of law, to attempt to employ the teachings of Pintchovski et al. in rejecting any of Applicant's claims.

Brigham et al. explicitly teach (Figs 2a-2c and 3a-3d) formation of "reox" oxide layer 24 or 34, completely surrounding the gate electrode. Further, Brigham et al. teach (Background; cols. 3-9) that the "reox" layer is critical to formation of high performance transistors.

Claims 44, 48, 49, 51 and 52 variously depend from Applicant's independent claims. As a result, these claims incorporate the recitation of the associated independent claims by reference (35 U.S.C. 112, 4TH ¶) As noted above with respect to Hiroki et al., none of these claims are compatible with these teachings.

As a result, not only do Brigham et al. explicitly teach away from the invention as recited in any of Applicant's claims, but the intended purpose of Brigham et al. is destroyed in attempting to modify the teachings of Brigham et al. to try to arrive at the subject matter of Applicant's claims. As a result, there is no motivation, as a matter of law, to attempt to

employ the teachings of Brigham et al. in rejecting any of Applicant's claims.

Kumagai et al. teach (Background) that short channel LDD MOSFETs have difficulty forming inversion regions rapidly and thus are limited in current carrying capability and are difficult to provide adequate drive signals to. As a result, Kumagai et al. teach (Abstract; Summary; embodiments described in Detailed Description) the benefits of using a sidewall spacer immediately adjacent the gate electrode that has a higher dielectric constant than the gate. This configuration concentrates electrical flux into an area where the transistors taught by Kumagai et al. benefit therefrom.

This benefit is completely destroyed in adapting the teachings of Kumagai et al. to try to arrive at the invention as recited in any of Applicant's claims because the dielectric constant resulting from oxidation of Kumagai et al.'s polysilicon gate material 12 is much lower than that of the high dielectric constant sidewall structures taught by Kumagai et al. and in fact is comparable to the dielectric constant of the gate dielectric taught by Kumagai et al. Accordingly, there is no motivation, as a matter of law, to attempt to modify the teachings of Kumagai et al. to try to arrive at the subject matter of any of Applicant's claims.

For at least these reasons, the rejections of all of Applicant's claims are prima facie defective and should be withdrawn, and claims 41 and 43-52 should be allowed.

New claim 53 is supported at least by text appearing at p. 4, line 5 through p. 11, line 5 of the specification as originally filed. No new matter is added by new claim 53. New claim 53 distinguishes over the art of record and is allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

Applicant respectfully asserts that claims 41 and 43-53 are in condition for allowance. Action to that effect is earnestly sought. If, however the Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic interview. The undersigned is available during normal business hours, Pacific Coast Time.

Respectfully submitted,

Dated: March 4, 2002 By: _____
Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/059,644
Filing Date ..... April 13, 1998
Inventor ..... Pai-Hung Pan
Assignee ..... Micron Technology, Inc.
Group Art Unit 2822
Examiner ..... M. Trinh
Attorney's Docket No. MI22-898
Title: Semiconductor Processing Methods of Forming a Conductive Gate and Line

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii)
FILING REQUIREMENTS TO ACCOMPANY RESPONSE TO DECEMBER 27, 2001 FINAL OFFICE ACTION
RESPONSE TO ACCOMPANY RCE FILING

Underlines indicate insertions and brackets indicate deletions.

In the Specification

On page 28, the paragraph extending from line 1 to line 19 has been amended as shown below:

ABSTRACT OF THE DISCLOSURE

A semiconductor processing method of forming a conductive gate or gate line over a substrate includes, a) forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls and an interface with the gate dielectric layer; b) electrically insulating the gate sidewalls; and c) after electrically insulating the gate sidewalls, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate interface with the gate dielectric layer. According to one aspect of the invention, the step of exposing the substrate to oxidizing conditions is conducted after provision of a first insulating material and subsequent anisotropic etch thereof to insulate the gate sidewalls. [According to another aspect of the invention, the step of exposing the substrate to oxidizing conditions is conducted after provision of first and second insulating materials and subsequent anisotropic etch thereof to insulate the gate sidewalls. According to another aspect of the invention, the step of exposing the substrate to oxidizing conditions is conducted after provision and subsequent anisotropic etch of a first insulating material, followed by provision and subsequent anisotropic etch of a second insulating material.]

In the Claims

41. (Fourfold amended) A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a conductive gate electrode over a gate dielectric layer on a substrate, the gate electrode having sidewalls and an interface with the gate dielectric layer;

forming sidewall spacers comprising nitride on the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer; and

after forming the sidewall spacers comprising nitride [and prior to forming source/drain regions], exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith, wherein a [potion] portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, is oxidized.

44. (Twice amended) The method of claim 41, wherein the forming of the sidewall spacers includes:

depositing a first material over the gate electrode;

depositing a second material over the first material; and

anisotropically etching the first and second materials to a degree sufficient to leave the spacers over the gate's sidewalls, the spacers being defined by both the first and second material.

45. (Fourfold amended) A semiconductor processing method of forming a conductive gate comprising:

forming a conductive gate structure on a first layer which is disposed on a substrate, the gate structure comprising a gate electrode having sidewalls and an interface with the first layer;

forming sidewall spacers laterally adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprising the sidewalls, the sidewall spacers comprising an oxidation resistant material; and

after forming the oxidation resistant sidewall spacers [and prior to forming source/drain regions adjacent the gate structure], conducting an oxidizing step by channeling oxidants through the first layer which is outwardly exposed laterally proximate the oxidation resistant sidewall spacers wherein the oxidation resistant sidewall spacers provide that only a portion of the gate electrode, adjacent the oxidation resistant sidewall spacers and at the interface with the first layer, is oxidized.

50. (Fourfold amended) A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a dielectric layer on a substrate;

forming a conductive gate structure over the dielectric layer, the gate structure having sidewalls defining a lateral dimension of the gate structure;

forming non-oxide material over the gate structure and the dielectric layer;

anisotropically etching the non-oxide material to form spacers on the sidewalls, the spacers laterally adjacent the gate structure and joining with the gate dielectric layer there at; and

[prior to forming source/drain regions,] exposing the substrate to oxidizing conditions effective to oxidize only that portion of the gate structure adjacent the spacers and the dielectric layer.

52. (Fourfold amended) A semiconductor processing method of forming a conductive gate comprising:

forming a gate structure atop a substrate having a dielectric layer thereon, at least a portion of the gate structure being conductive, the conductive portion comprising:

a polysilicon layer,

an overlying metal, and

a reaction barrier layer interposed between the polysilicon and the overlying metal;

covering a top and sidewalls of the gate structure with an oxidation resistant material, said covering comprising:

a first barrier material contacting the sidewalls, and

a second barrier material disposed over the first barrier material,

anisotropically etching the oxidation resistant material to a degree sufficient to leave the oxidation resistant material laterally adjacent to and covering all of the sidewalls of the gate structure while exposing the dielectric layer adjacent the gate structure; and

[prior to forming source/drain regions proximate the gate structure,] exposing the substrate to oxidation conditions effective to oxidize a portion of the gate structure laterally adjacent the covered sidewalls and adjacent the dielectric layer.

New claim 53 has been added.

END OF DOCUMENT